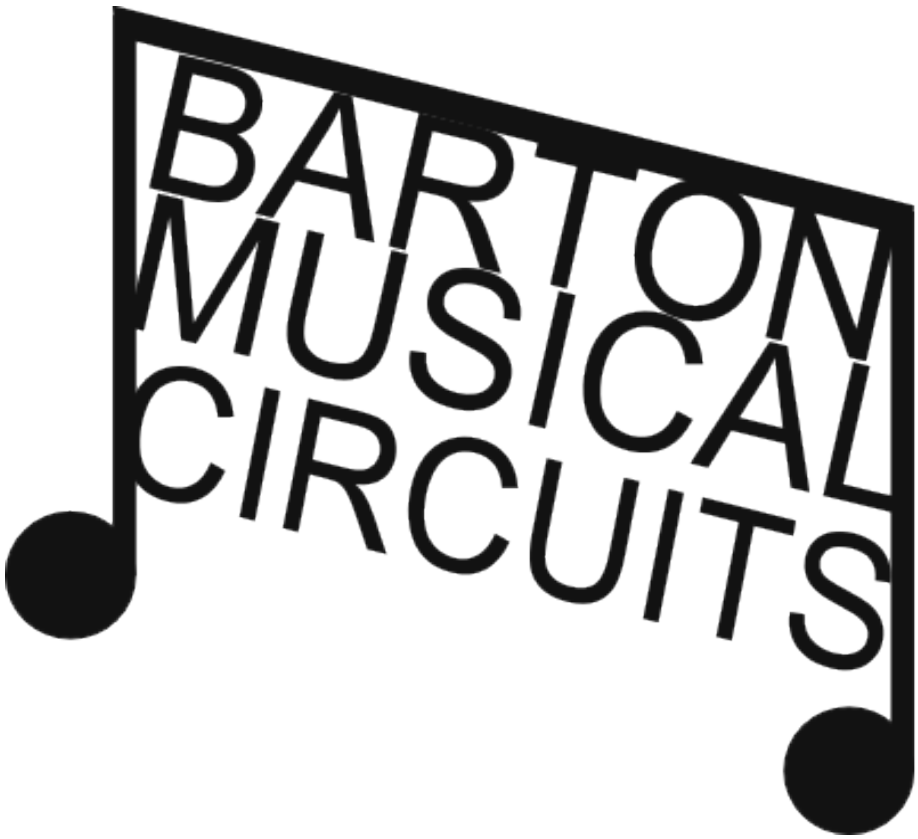


BMC 077. 4HP Parallel digital to analog converter (DAC) Build Documentation.

I. Using The Module
II. Schematic
III. Construction
A. Parts List
B. PCB Layout

I. Using The Module.

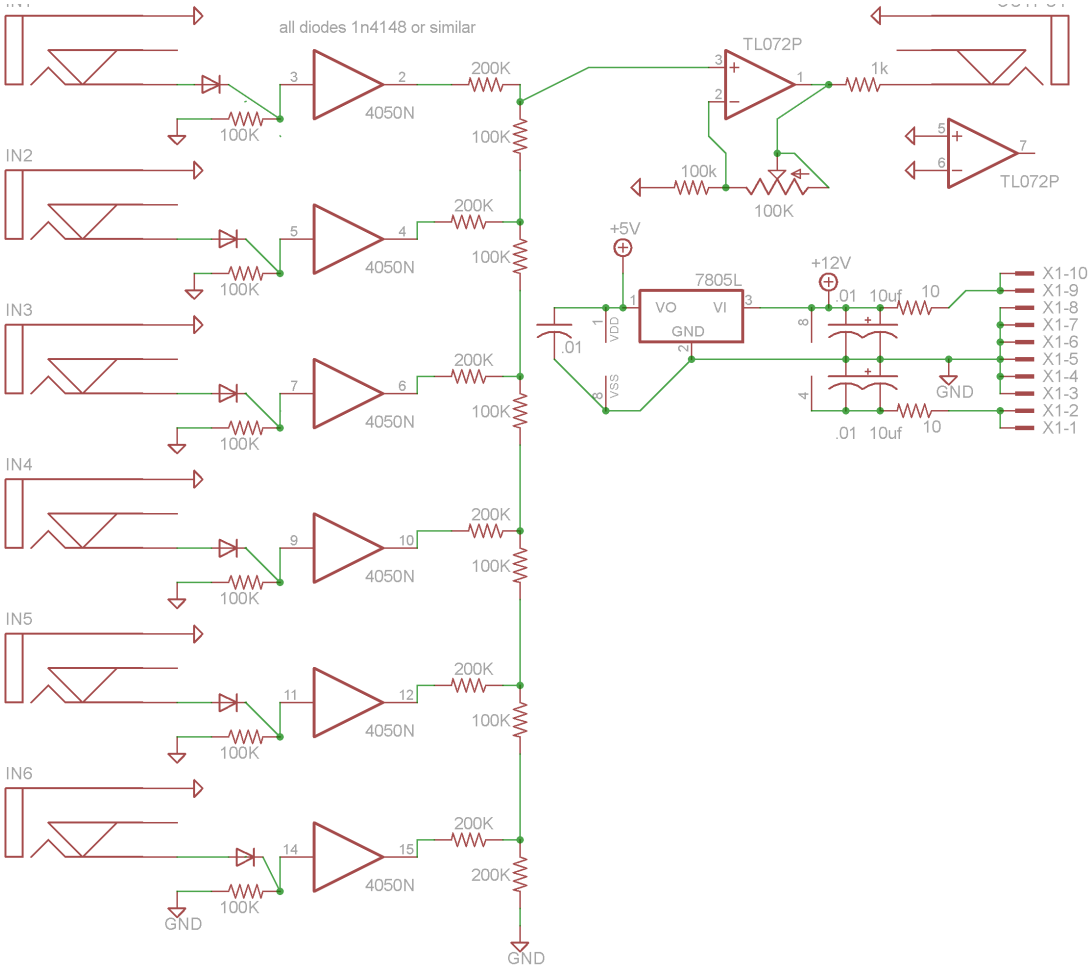
This module is a 6-bit digital to analog converter with parallel inputs. Each of the six inputs corresponds to a bit in a binary number with the top input being the most-significant bit and the bottom input being the least-significant bit. The output is an analog voltage that corresponds to the binary number formed by the inputs.

This means that each input raises output voltage by twice as much as the previous input did. In my testing I've calibrated it so that the least-significant bit was $1/12^{th}$ of a volt (0.0834V) so that when the output is fed into a 1V/oct input on an oscillator it was a musical semi-tone, the next input a full-tone and the next two full tones, etc.

The module is designed for +5V gate/trigger inputs or +/-5V LFO inputs. Inputting voltages over +5V can raise the output voltage, causing inaccuracies.

CALIBRATION OPTIONS

Step 1: Decide how much change in output you'd like when increasing the binary number by 1. Increasing the output by 1 is the same as inputting a gate to the least-significant bit input. If you have a maximum output voltage in mind, you can divide that maximum voltage by 64 to determine voltage change.
Step 2: Input a gate to Input 6, the least-significant input. Measure the voltage on the output.
Step 3: Adjust the cermet pot until the output is equal to the desired voltage.



II. Schematic.

Above is the schematic for this module. The input jacks are on the left with the most-significant bit input labeled ”In1” and the least-significant bit input labeled “In6” The tip of each input jack goes through a 1N4148 diode to only allow positive voltage to pass. This connects to the input of a CD4050 buffer IC with 100K pull-down resistors to ground the inputs when no voltage is passed through the diode.

The outputs of the CD4050 are connected to an R/2R ladder composed of 100K and 200K resistors. This configuration of resistors is where the actual change from digital to analog happens. The CD4050 is powered by a 78L05 +5V regulator, so it's outputs will only ever be 0V or +5V making for a clean signal for the R/2R ladder.

The output of the R/2R ladder connects to an op-amp wired as a non-inverting amplifier. In the feedback path of the amplifier is the 100K cermet pot used for calibrating the circuit. Increasing the resistance of the cermet pot will increase the output voltage and lowering it will lower the output voltage. A 1K resistor connects to the output jack.

If you wanted to calibrate to an even smaller voltage range, you could increase the value of the 100K resistor to ground that connects to pin 7 of the op-amp. To achieve a larger output range, make this resistor a smaller value.

The power connector connects the +-/12V voltage rails through 10 ohm resistors, these form a low pass filter with the 10uf capacitors on board. Additional filtering is provided by .01uf capacitors near the power pins of ICs. A +5V supply for the CD4050 is supplied by a 78L05 regulator

III. Construction
A. Parts List

Semiconductors

Value	Quantity	Notes
TL072	1	8 pin DIP
CD4050	1	16 pin DIP
1N4148	6	Or other small switching diode
78L05	1	TO-92 package

Resistors

Value	Quantity	Notes
10 ohm	2	5mm lead spacing. Use 3.5mm body length or stand up
1Kohm	1	" "
100 Kohm	12	" "
200 Kohm	7	" "
100 Kohm Cermet pot	1	64W package

Capacitors

Value	Quantity	Notes
.01uf	3	Small ceramic disc. Value not critical
10uf	2	Electrolytic

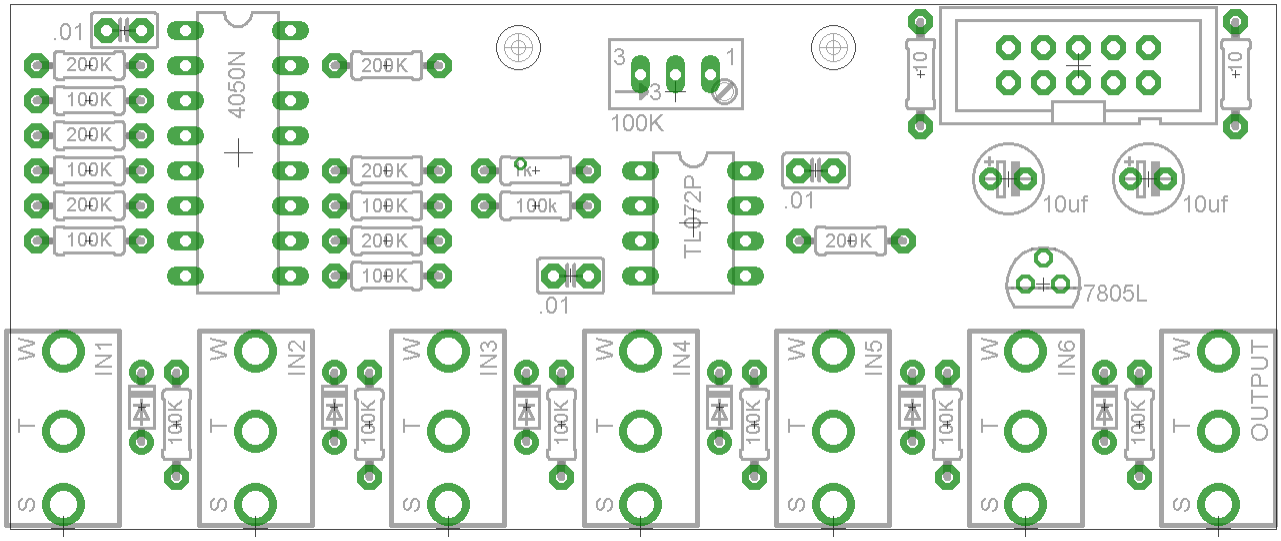
Other/Off Panel

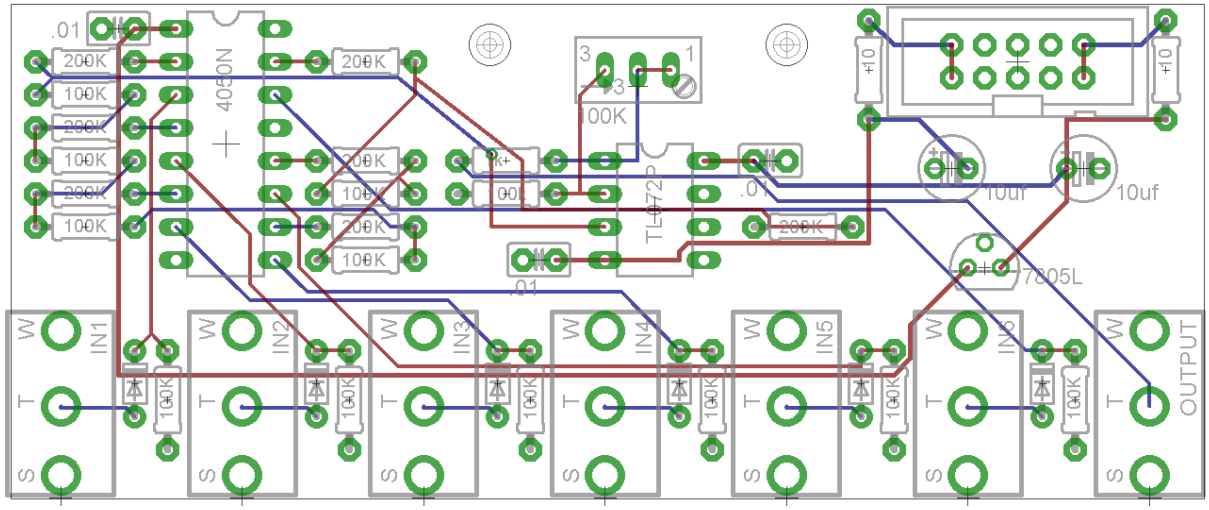
Value	Quantity	Notes
Power connecter	1	Right angle 2x5 2.54mm, like this.
Jacks	7	PCB is designed around these jacks: PJ-323M
8 pin DIP Socket	1	
16 pin DIP socket	1	

B. PCB Layout

Below are renderings of the PCB. The rendering showing the traces does not show the ground fill plane, so assume any missing connection is a ground fill.

The PCB measures 92mm x 38mm and the jacks are spaced 14mm apart.





This is a photo of a completed module